

Figure 1 (PRIOR ART)

Cross-section of a trenched DMOS power transistor cell (prior art, /1,2/).

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Figure 2,a (PRIOR ART)

"Open-cell" implementation of a trenched DMOS power transistor (CALMA hard copy, active region). Siliconix, Inc., 1987.

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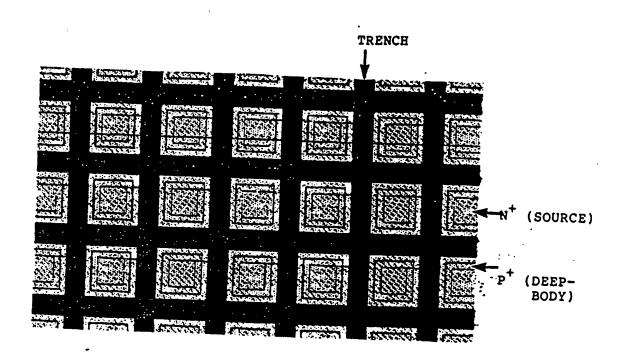
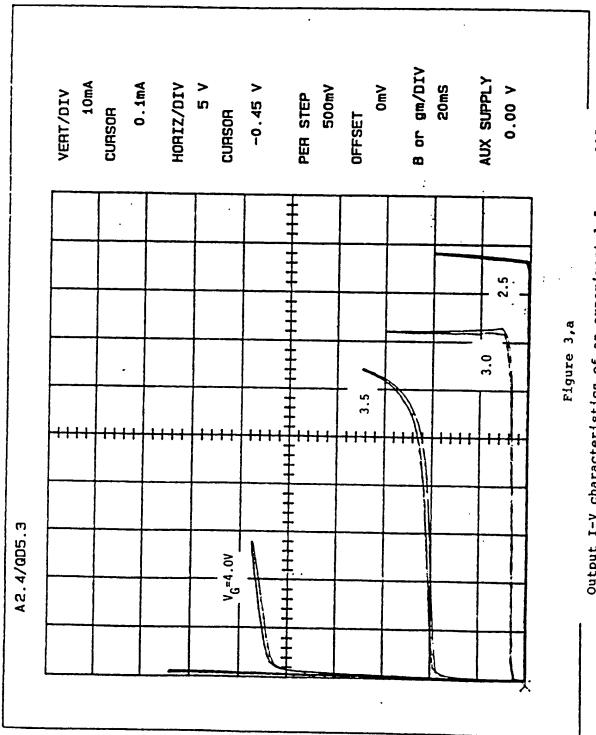


Figure 2,b (PRIOR ART)

"Closed-cell" implementation of a trenched DMOS power transistor (CALMA hard copy, active region). Siliconix, Inc., 1987.

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Output I-V characteristics of an experimental "open-cell" trenched DMOS transistor having distant body contacts, perpendicular to the trenches. Siliconix, Inc., 1988.

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B or gm/DIV AUX SUPPLY 20mS 0.1mA 10mA 500mV **O⊞** S > -0.15 V 0.00 V HORIZ/DIV Output I-V characteristics of an experimental "open-cell" trenched DMOS transistor having closely-spaced body contacts, perpendicular to the trenches. Siliconix, Inc., 1988. PER STEP VERT/DIV CURSOR CURSOR OFFSET 3.0 (PRIOR MET) Figure 3,b A2.1/0D5.3 V₆=4.5V

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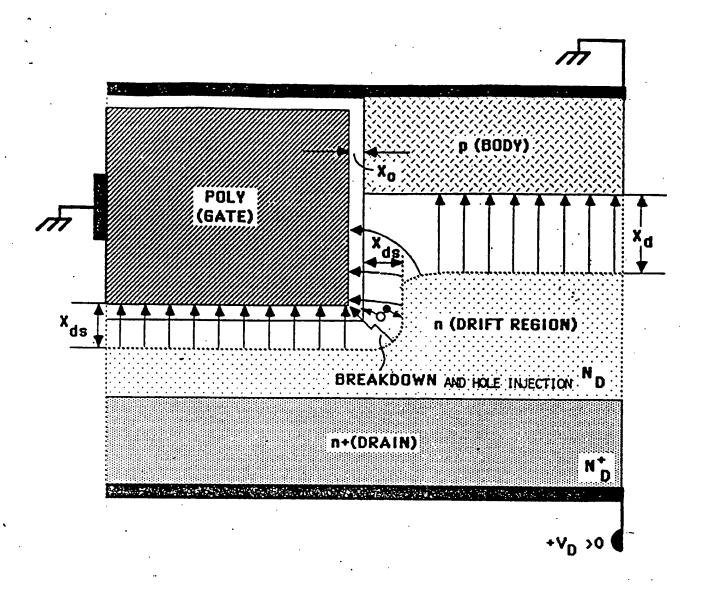


Figure 4 (PRIOR ART)

Qualitative description of the electric-field structure in a trenched DMOS transistor having no deep-body profile provision. BVDSS biasing, source junction omitted.

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POTENTIAL (dV=5V) AND FIELD LINES, VD=50V, D10

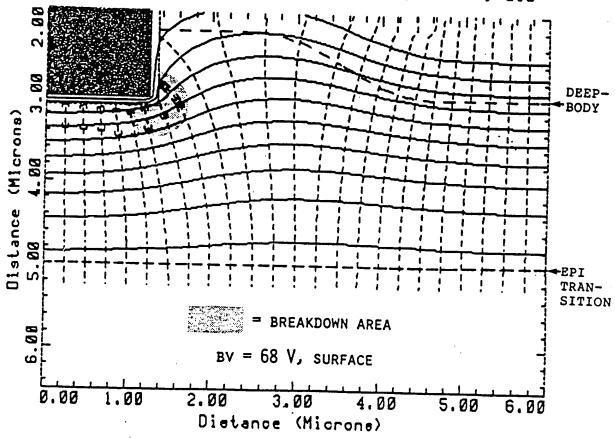


Figure 5 (PRIOR ART)

2-D computer simulation of the BVDSS operation of a trenched DMOS transistor having the deep body junction shallower than the trench.

Drain breakdown takes place beneath the trench surface.

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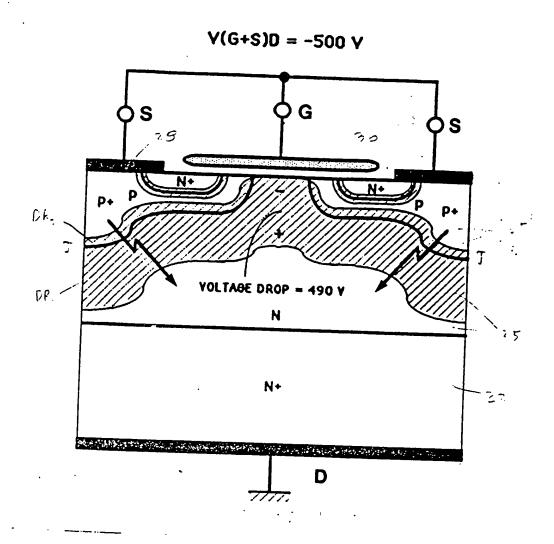


Figure 6 (PRIOR ART)

Junction and depletion-region topology of a planar DMOS transistor biased in the BVDSS condition.

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2-D OXIDATION SQUARE-CELL DESIGN

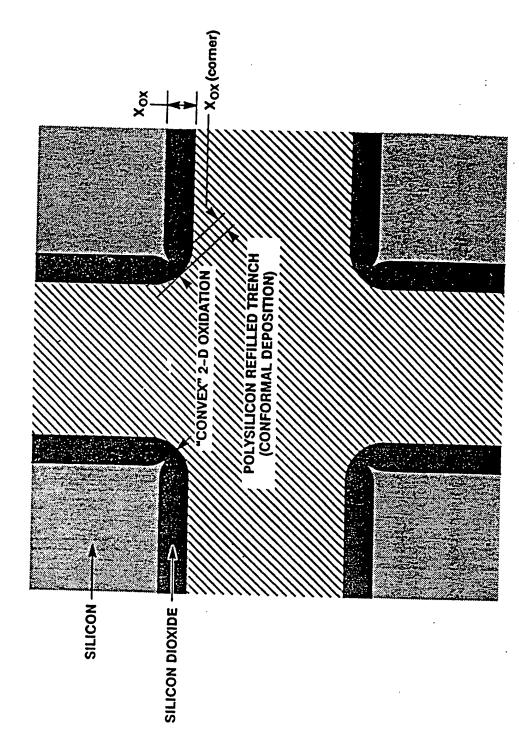


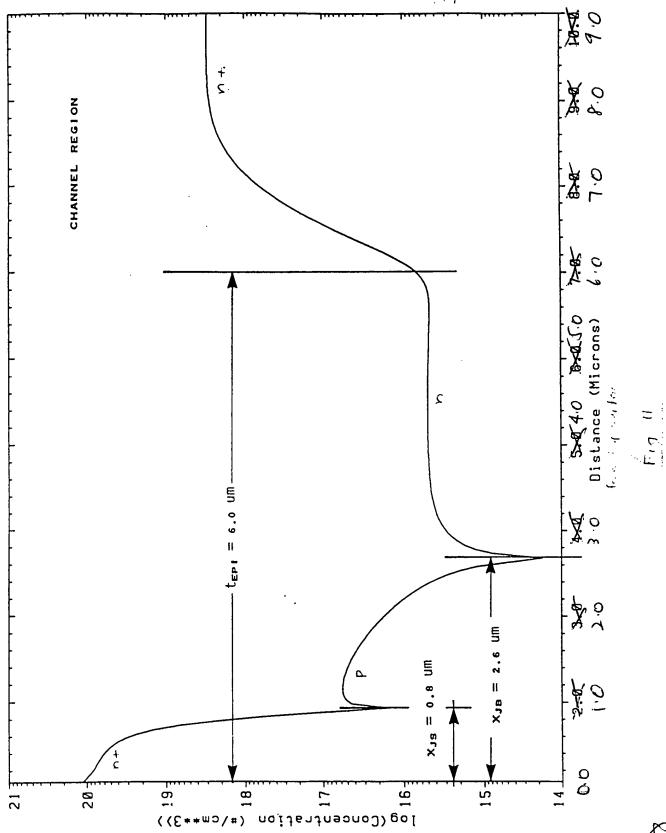
Figure 7 (PRIOR ACT)

Qualitative description of the oxide profile at a rectangular trench intersection.

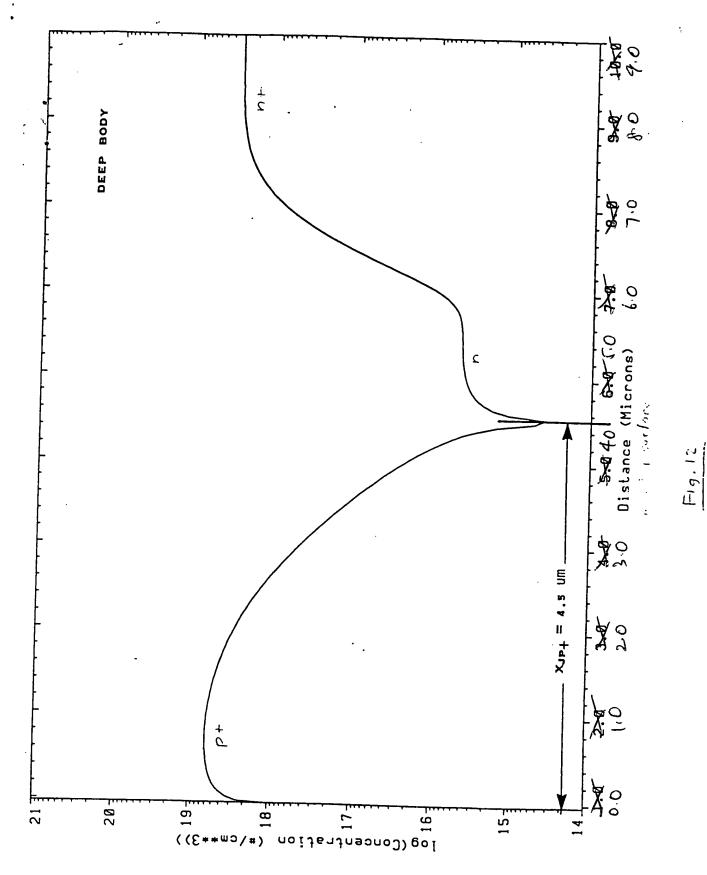
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